19-3584; Rev 0; 2/05

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

General Description

The MAX5079 ORing MOSFET controller replaces ORing diodes in high-reliability redundant, parallel-connected power supplies. Despite their low forward-voltage drop, ORing Schottky diodes cause excessive power dissipation at high currents. The MAX5079 allows for the use of low-on-resistance n-channel power MOSFETs to replace the Schottky diodes. This results in low power dissipation, smaller size, and elimination of heatsinks in high-power applications.

The MAX5079 operates from 2.75V to 13.2V and includes a charge pump to drive the high-side n-channel MOSFET. Operation down to 1V is possible if an auxiliary voltage of at least 2.75V is available. When the controller detects a positive voltage difference between IN and BUS, the n-channel MOSFET is turned on. The MOSFET is turned off as soon as the MAX5079 sees a negative potential at IN with respect to the BUS voltage, and is automatically turned back on when the positive potential is restored. Under fault conditions, the ORing MOSFET's gate is pulled down with a 1A current, providing an ultra-fast 200ns turn-off. The reverse voltage turn-off threshold is externally adjustable to avoid unintentional turn-off of the ORing MOSFET due to glitches at IN or BUS caused by hot plugging the power supply.

Additional features include an OVP flag to facilitate shutdown of a failed power supply due to an overvoltage condition, and a PGOOD signal that indicates if V_{IN} is either below the undervoltage lockout or V_{BUS} is in an overvoltage condition. The MAX5079 operates over the -40°C to +85°C temperature range and is available in a space-saving 14-pin TSSOP package.

Applications

Paralleled DC-DC Converter Modules

N+1 Redundant Power Systems

Servers

Base-Station Line Cards

RAID

Networking Line Cards

Pin Configuration appears at end of data sheet.

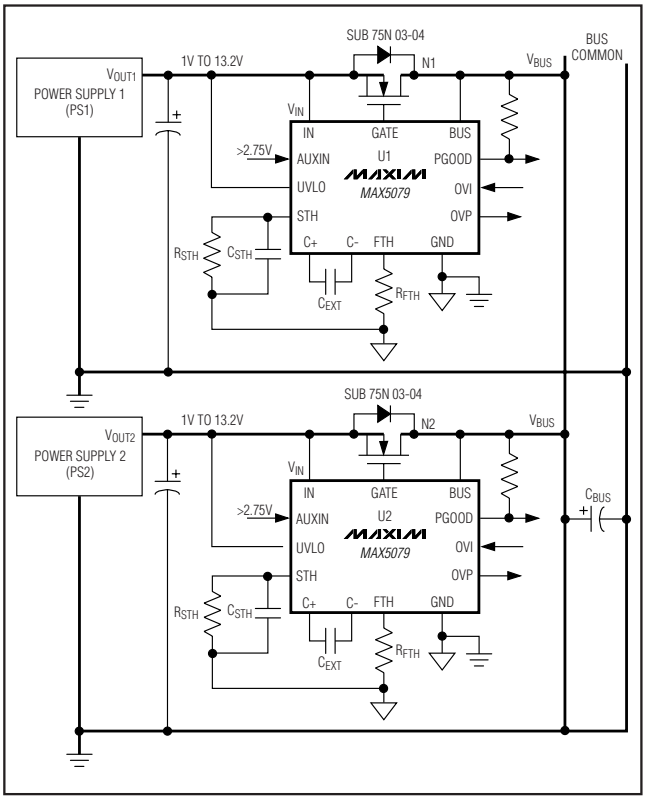
Features

- **2.75V to 13.2V Input ORing Voltage**
- **1V to 13.2V Input ORing Voltage with 2.75V Aux Voltage Present**
- **2A MOSFET Gate Pulldown Current During Fault Condition**
- **Ultra-Fast 200ns, MOSFET Turn-Off During Fault Condition**
- **Supply Undervoltage and Bus Overvoltage Detection**
- **Power-Good (PGOOD) and Overvoltage (OVP) Outputs for Fault Detection**
- **Space-Saving 14-Pin TSSOP Package**
- **-40°C to +85°C Operating Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5079EUD	-40°C to +85°C	14 TSSOP

Typical Operating Circuit



ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

ABSOLUTE MAXIMUM RATINGS

GATE to GND .....-0.3V to (V_{IN} + 8.5V)
All Other Pins to GND.....-0.3V to +15V
Continuous Current Into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727.3mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

((V_{IN} = 2.75V to 13.2V and V_{AUXIN} = 0V) or (V_{IN} = 1V and V_{AUXIN} = 2.75V to 13.2V), R_{STH} = open, R_{FTH} = 0, V_{UVLO} = 1V, V_{OVI} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V and T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
IN Input Voltage Range	V_{IN}		2.75		13.20	V
		$V_{AUXIN} \geq 2.75V$	1.0		13.2	V
AUXIN Input Voltage Range	V_{AUXIN}		0		13.2	V
(V_{AUXIN} - V_{IN}) High Threshold (When GATE Connects Directly to AUXIN) (Note 2)	$V_{AUXIN\_THRESHOLD}$	V_{AUXIN} rising, I_{GATE} = 10µA	4.3	4.9	5.4	V
(V_{AUXIN} - V_{IN}) Hysteresis (When GATE Connects Directly To AUXIN)	$V_{AUXIN\_HYSTERESIS}$			40		mV
IN Supply Current	I_{IN}	V_{UVLO} = 1V, $V_{IN} > V_{BUS}$			4	mA
AUXIN Leakage Current	I_{LEAK_AUX}	V_{AUXIN} = 0V			20	µA
AUXIN Supply Current	I_{AUXIN}	V_{UVLO} = 1V, V_{AUXIN} = 13.2V, $V_{AUXIN} \geq V_{IN}$, $V_{AUXIN} \geq V_{BUS}$			4	mA
BUS Leakage Current	I_{LEAK_BUS}	V_{IN} = 13.2V, V_{BUS} = 0V			1	mA
BUS Supply Current	I_{BUS}	V_{BUS} = 13.2V, $V_{BUS} > V_{IN}$, $V_{BUS} > V_{AUXIN}$			3	mA
IN TO AUXIN SWITCHOVER						
Switchover High Threshold	V_{AUXIN_HIGH}	(V_{IN} - V_{AUXIN}), V_{AUXIN} falling	-60	+25	+200	mV
Switchover Low Threshold	V_{AUXIN_LOW}	(V_{IN} - V_{AUXIN}), V_{AUXIN} rising	-200	-25	+50	mV
IN UNDERVOLTAGE LOCKOUT						
Internal UVLO High Threshold	$V_{INTUVLO\_HIGH}$	V_{IN} rising, V_{AUXIN} = 0V or V_{AUXIN} rising, V_{IN} = 0V	2.0	2.25	2.5	V
Internal UVLO Hysteresis	$V_{INTUVLO\_HYST}$	V_{IN} falling, V_{AUXIN} = 0V or V_{AUXIN} falling, V_{IN} = 0V		30		mV
External UVLO Threshold	V_{UVLO}	V_{UVLO} falling	0.568	0.6	0.632	V
External UVLO Hysteresis	V_{UVLO_HYST}			60		mV
External UVLO Input Bias	I_{UVLO}				500	nA

ELECTRICAL CHARACTERISTICS (continued)

((V_{IN} = 2.75V to 13.2V and V_{AUXIN} = 0V) or (V_{IN} = 1V and V_{AUXIN} = 2.75V to 13.2V), R_{STH} = open, R_{FTH} = 0, V_{UVLO} = 1V, V_{OVI} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V and T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ORing MOSFET CONTROL						
ORing MOSFET Turn-On Time	t_{ON}	C_{GATE} = 10nF, C_{EXT} = 100nF, MOSFET gate threshold = 2V		10	25	µs
ORing MOSFET Forward Voltage Threshold (Fast Comparator)	V_{DTH}	(V_{IN} - V_{BUS}) rising	5	12.5	20	mV
ORing MOSFET Reverse Voltage Turn-Off Threshold (Fast Comparator (V_{IN} - V_{BUS}))	V_{FTH}	R_{FTH} = 0	-12	-24	-31	mV
		R_{FTH} = 12kΩ	-63	-104	-150	
		R_{FTH} = 27kΩ, V_{IN} ≥ 3.5V	-126	-204	-300	
ORing MOSFET Reverse Voltage Blanking Time (Fast Comparator)	t_{FBL}	V_{BUS} = 2.8V, R_{FTH} = 0, V_{BUS} - V_{IN} = 0.3V		50		ns
Slow-Comparator Output Voltage Threshold on STH	V_{O_STH}		0.95	1	1.05	V
ORing MOSFET Reverse Voltage Turn-Off Threshold (Slow Comparator (V_{IN} - V_{BUS}))	V_{STH}	R_{STH} open	-0.1	-12	-24.0	mV
		R_{STH} = 500kΩ		-25		
		R_{STH} = 64kΩ		-100		
(V_{IN} - V_{BUS}) to I_{STH} Transconductance (Slow Comparator)	G_{M_STH}	V_{STH} = 0V		0.17		mS
ORing MOSFET Reverse Voltage Blanking Time (Slow Comparator)	t_{SBL}	STH floating	0.5	0.9	1.5	ms
		C_{STH} = 0.047µF		5		
		C_{STH} = 0.22µF		14		
ORing MOSFET DRIVER						
Gate-Charge Current	I_{GATE}	C_{EXT} = 100nF	0.7	2		mA
Gate Discharge Current (Note 3)	$I_{GATE.DIS\_MIN}$	V_{GATE} ≥ V_{IN}, V_{IN} = 5V, V_{BUS} = 5V	0.9	2	5.0	A
		V_{GATE} ≥ V_{IN}, V_{IN} = 2.75V, V_{BUS} = 3.5V		1.3		
		V_{GATE} ≥ V_{IN}, V_{IN} = 12V, V_{BUS} = 13.2V		3.2		
Gate Fall Time	t_{FGATE}	V_{BUS} = 3.5V, C_{GATE} = 0.1µF		600		ns
		V_{BUS} = 3.5V, C_{GATE} = 0.01µF		200		
Gate Discharge Current Delay Time (Time from V_{IN} Falling from 3.7V to 3V to V_{GATE} = V_{IN})	t_{DIS_GATE}	V_{BUS} = 3.5V, V_{FTH} = 0V, C_{GATE} = 0.1nF		70	200	ns
Gate to IN Resistance	R_{GATE_IN}	(V_{GATE} - V_{IN}) = 100mV			900	Ω
Gate to IN Clamp Voltage	$V_{GATE\_IN\_CLAMP}$	I_{GATE} = 10mA, V_{IN} ≥ V_{BUS}	8.5		11	V
Gate-Drive Voltage (Measured with Respect to V_{IN})	(V_{GATE} - V_{IN})	2.7V < V_{IN} < 13.2V	3.8			V
		V_{IN} = 13.2V	6.5	7	7.6	
		V_{IN} = 2.75V	4.5	5	5.5	
V_{IN} Switchover Threshold to Higher GATE Voltage (Note 4)	V_{IN_SOTH+}		7.4	8	8.5	V

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

ELECTRICAL CHARACTERISTICS (continued)

((VIN = 2.75V to 13.2V and VAUXIN = 0V) or (VIN = 1V and VAUXIN = 2.75V to 13.2V), RSTH = open, RFTH = 0, VUVLO = 1V, VOVI = 0V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at VIN = 12V and TA = +25°C. See the *Typical Operating Circuit*.) (Note 1)

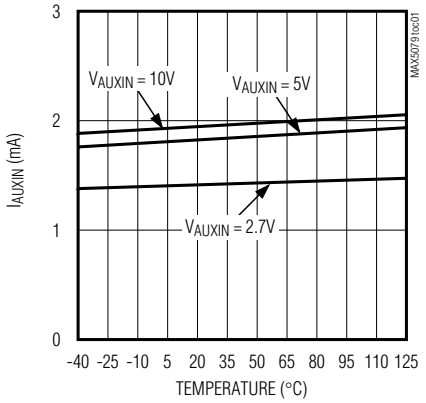
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIN Switchover Hysteresis (Note 4)	VIN_SOHYS			40		mV
Charge-Pump Frequency	fCP	External		70		kHz
		Internal, VIN < 5V, VAUXIN < 5V		1100		
PROTECTION						
OVI Input Bias Current	IOVI				500	nA
OVI Threshold	VOVI_TH	OVI rising	0.568	0.6	0.632	V
OVP Output Low Voltage	VOVP_LOW	VOVI = 1V, ISINK = 10mA		0.2	0.4	V
OVP Leakage Current	IOVP_LEAK	VIN = 2.75V, VOVP = 13.2V			1	µA
PGOOD Leakage Current	IPG_LEAK	VPGOOD = 13.2V			1	µA
PGOOD Output Low Voltage	VPG_LOW	ISINK = 2mA		0.2	0.4	V

Note 1: All devices are production tested at +25°C. Limits over temperature are guaranteed by design.
Note 2: Threshold is reached when charge pump turns off.
Note 3: Gate discharge current is guaranteed through the testing of gate fall time.
Note 4: VIN switchover threshold is VIN at which the gate-drive voltage (VGATE - VIN) goes from 5V to 7V, VIN rising and (VIN ≥ VBUS).

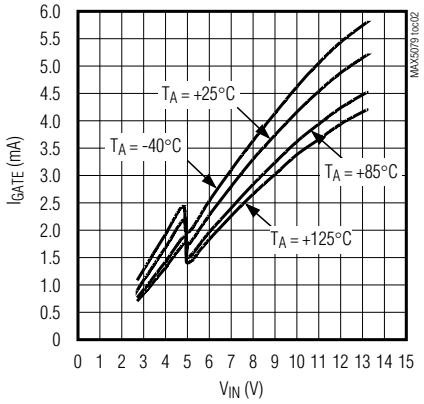
Typical Operating Characteristics

(TA = +25°C, unless otherwise noted. See the *Typical Operating Circuit*.)

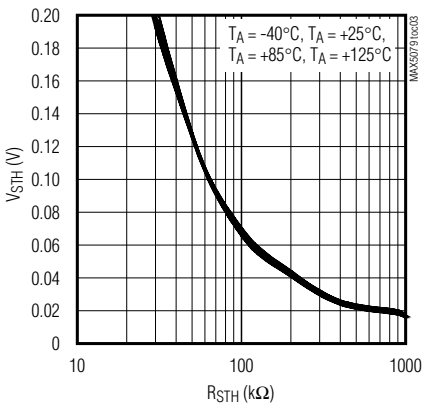
AUXIN SUPPLY CURRENT vs. TEMPERATURE (VIN = VBUS = 1V)



GATE-CHARGE CURRENT vs. VIN



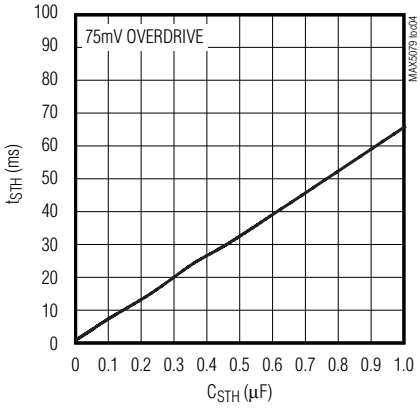
SLOW-COMPARATOR REVERSE VOLTAGE THRESHOLD (VSTH vs. RSTH)



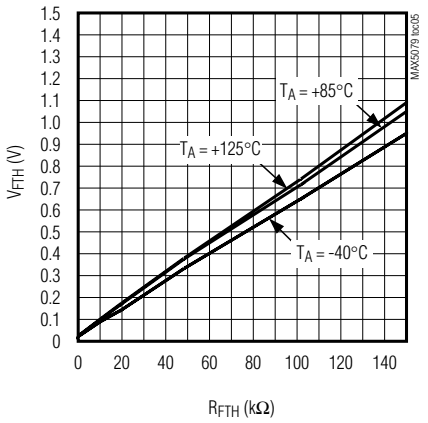
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. See the *Typical Operating Circuit*.)

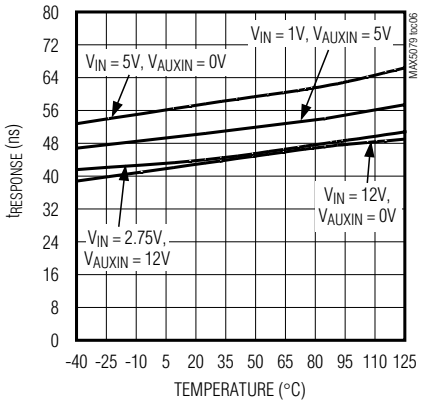
SLOW-COMPARATOR BLANKING TIME t_{STH} vs. C_{STH} (R_{STH} = 180kΩ)



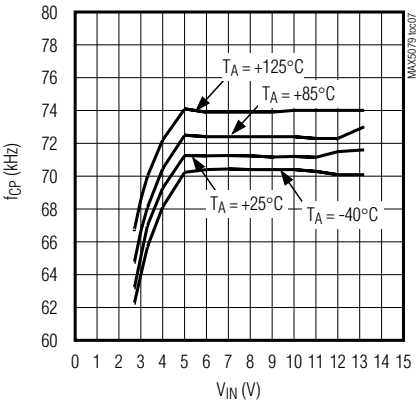
FAST-COMPARATOR REVERSE VOLTAGE THRESHOLD (V_{FTH} vs. R_{FTH})



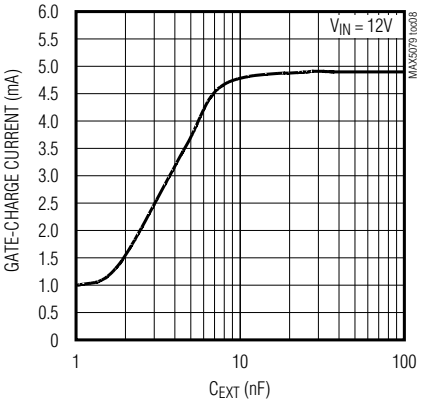
FAST-COMPARATOR RESPONSE TIME



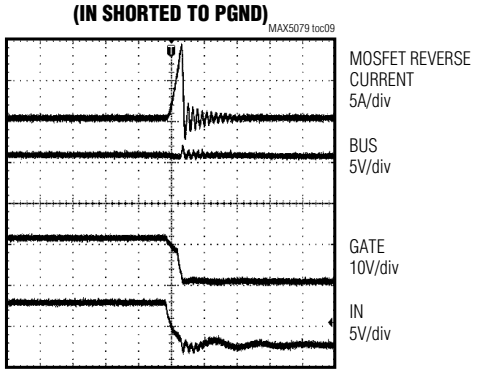
CHARGE-PUMP FREQUENCY vs. INPUT VOLTAGE



GATE-CHARGE CURRENT vs. C_{EXT}



FAULT CURRENT WAVEFORM (IN SHORTED TO PGND)



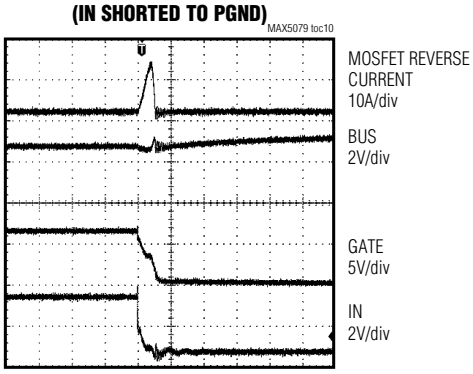
VIN = 5V, VBUS = 5V,
VAUXIN = 0V, CSTH = 0,
RSTH = OPEN, RFTH = 0,
UVLO = IN

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

Typical Operating Characteristics (continued)

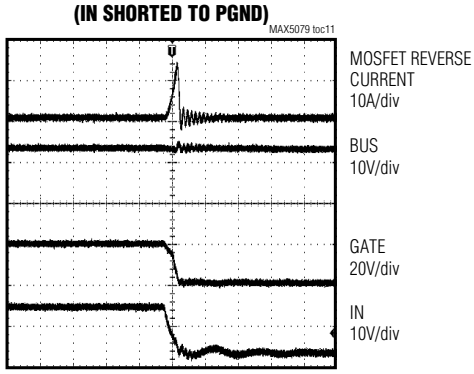
(T_A = +25°C, unless otherwise noted. See the *Typical Operating Circuit*.)

FAULT CURRENT WAVEFORM (IN SHORTED TO PGND)



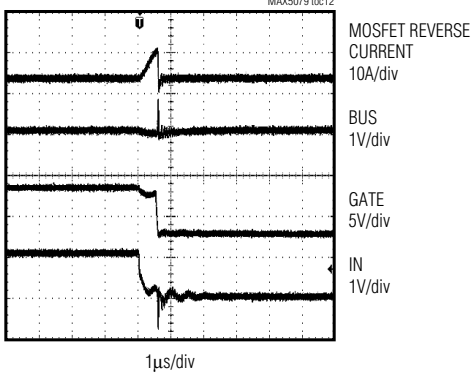
V_{IN} = 2.75V, V_{BUS} = 2.75V,
V_{AUXIN} = 0V, C_{STH} = 0µF,
R_{STH} = OPEN, R_{FTH} = 0,
UVLO = IN

FAULT CURRENT WAVEFORM (IN SHORTED TO PGND)



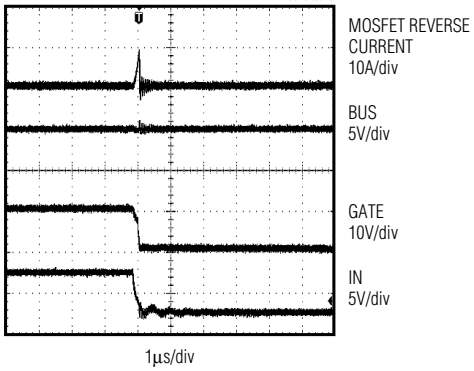
V_{IN} = 12V, V_{BUS} = 12V,
V_{AUXIN} = 0V, C_{STH} = 0µF,
R_{STH} = OPEN, R_{FTH} = 0,
UVLO = IN

FAULT CURRENT WAVEFORM (IN SHORTED TO PGND)



V_{IN} = 1V, V_{BUS} = 1V,
V_{AUXIN} = 5V, C_{STH} = 0µF,
R_{STH} = OPEN, R_{FTH} = 0,
UVLO = IN

FAULT CURRENT WAVEFORM (IN SHORTED TO PGND)

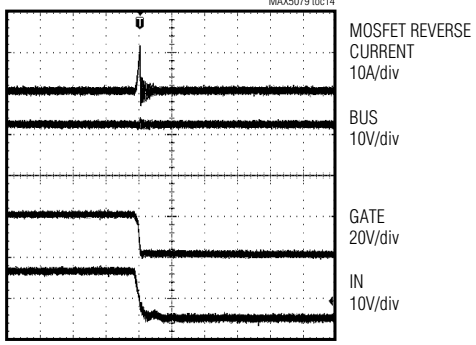


V_{IN} = 5V, V_{BUS} = 5V,
V_{AUXIN} = 5V, C_{STH} = 0µF,
R_{STH} = OPEN, R_{FTH} = 0,
UVLO = IN

Typical Operating Characteristics (continued)

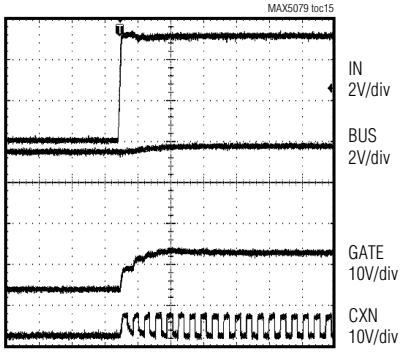
(T_A = +25°C, unless otherwise noted. See the *Typical Operating Circuit*.)

FAULT CURRENT WAVEFORM (IN SHORTED TO PGND)



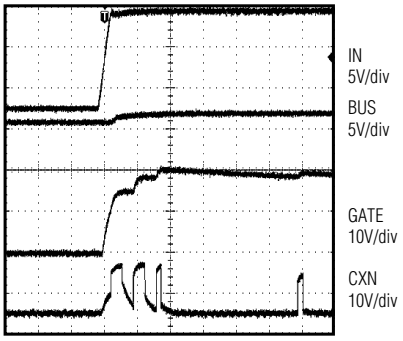
V_{IN} = 12V, V_{BUS} = 12V, V_{AUXIN} = 5V, C_{STH} = 0, R_{STH} = OPEN, R_{FTH} = 0, UVLO = IN

POWER-UP WAVEFORM



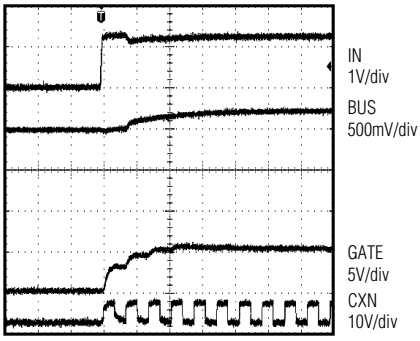
V_{IN} = 5.2V, V_{BUS} = 4.9V, I_{BUS} = 5A

POWER-UP WAVEFORM



V_{IN} = 12.2V, V_{BUS} = 11.9V, I_{BUS} = 5A

POWER-UP WAVEFORM



V_{IN} = 1.2V, V_{BUS} = 1V, V_{AUXIN} = 5V, I_{BUS} = 5A

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

Pin Description

PIN	NAME	FUNCTION
1	CXN	Negative Terminal of External Flying Charge-Pump Capacitor
2	CXP	Positive Terminal of External Flying Charge-Pump Capacitor
3	OVP	Open-Drain Active-Low Output. OVP sinks up to 10mA when $V_{OVI} \geq 0.6V$ and $V_{IN} \geq V_{BUS}$. OVP can be used to drive an optodiode. Cycle power or pull UVLO low and then high to reset OVP.
4	PGOOD	Open-Drain Active-Low Output. PGOOD pulls low when $V_{UVLO} \leq 0.6V$ or $V_{OVI} \geq 0.6V$.
5	STH	ORing MOSFET Slow-Comparator Reverse Voltage Threshold and Blanking Time Setting Input. Connect a resistor from STH to GND to set the threshold. Connect a capacitor from STH to GND to set the blanking time. Leave STH floating to set the internal threshold (-12mV) and internal blanking time (0.9ms).
6	FTH	Fast-Comparator Reverse Threshold Setting. Connect a resistor from FTH to GND to set the fast-comparator reverse voltage threshold from -24mV to -400mV.
7	OVI	Overvoltage Comparator Input. Connect OVI to BUS through a resistive divider.
8	UVLO	Undervoltage Lockout Comparator Input. Connect UVLO to IN through a resistive divider. The MAX5079 remains off until V_{UVLO} rises above 0.66V. When V_{UVLO} rises above 0.664V, V_{GATE} is raised to V_{IN}.
9	PGND	Power Ground. Ground discharge path of the 2A GATE pulldown. Connect to external power ground plane.
10	GATE	Gate-Driver Output for n-Channel ORing MOSFET
11	BUS	Bus Voltage-Sense Input. Connect BUS to the drain of the ORing MOSFET to sense the polarity of the Bus Current. The MAX5079 receives its power from BUS when V_{IN} and V_{AUXIN} are not present.
12	GND	Signal Ground. Connect to the low-level signal or analog ground.
13	IN	Source Connection for ORing MOSFET and Supply Input for the MAX5079. Connect IN directly to the power-supply voltage of 2.75V to 13.2V or 1V to 13.2V with $V_{AUXIN} \geq 2.75V$.
14	AUXIN	Auxiliary Power-Supply Input. AUXIN supplies power to the IC when $1V \leq V_{IN} \leq 2.75V$. Connect AUXIN to 2.75V or higher if V_{IN} is less than 2.75V.

Block Diagram

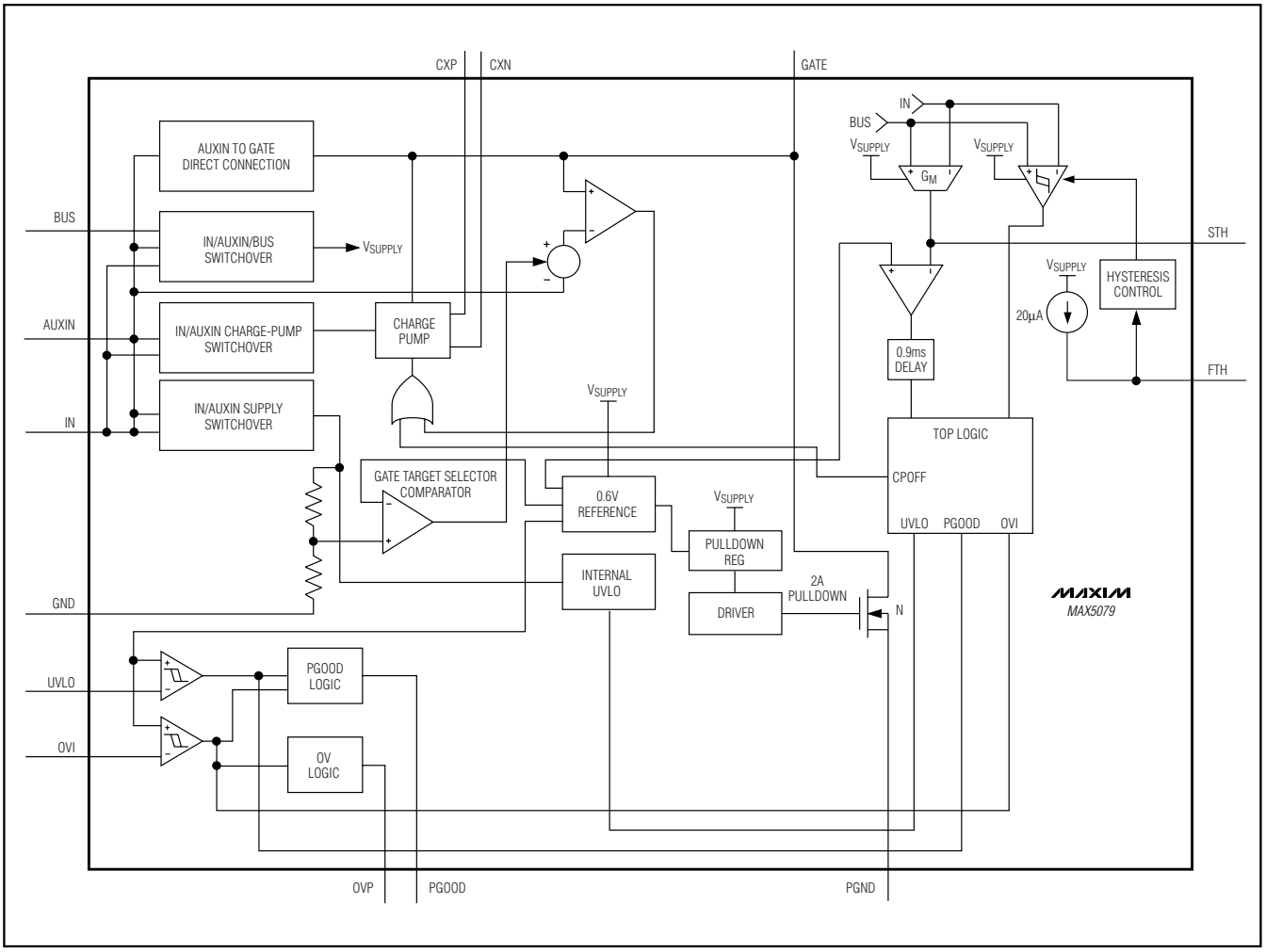


Figure 1. Block Diagram

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

Detailed Description

The MAX5079 ORing MOSFET controller drives an external n-channel MOSFET and replaces ORing diodes in high-reliability redundant power-management systems or multiple paralleled power supplies. The device has an internal charge pump to drive the high-side n-channel ORing MOSFET. Additional features include an adjustable undervoltage lockout threshold (UVLO), output overvoltage detector (OVI/OVP), input power-good detector (PGOOD), and two programmable reverse voltage detectors to detect both fast and slow rises in the reverse voltage across the ORing MOSFET. The input power-supply range is from 2.75V to 13.2V or down to 1V when an auxiliary supply of at least 2.75V is available.

Operational Description

This section describes a detailed startup sequence and behavior of the MAX5079 under different conditions of V_{BUS} and V_{IN}. The MAX5079 powers up whenever V_{IN} is equal to or greater than 2.75V and V_{UVLO} exceeds the UVLO threshold of 0.66V. Operation with V_{IN} down to 1V is possible as long as $V_{UVLO} \geq 0.6V$ and $V_{AUXIN} \geq 2.75V$.

When V_{UVLO} crosses the UVLO threshold, V_{GATE} rises to V_{IN} and the charge pump turns on. The charge pump delivers 2mA to charge the gate capacitance of the external MOSFET connected to GATE. The constant gate-charge current prevents large inrush currents from the input supply. During turn-on, the MAX5079 will ignore the reverse voltage at IN with respect to BUS. This is necessary to avoid the unintentional turn-off of the ORing MOSFET as the momentary inrush current causes V_{IN} to dip.

Figure 2 shows the MAX5079 in an ORing configuration with three parallel power supplies (PS1, PS2, and PS3) and three MAX5079s (U1, U2, and U3) provided by outputs V_{OUT1}, V_{OUT2}, and V_{OUT3}. The following events must be carefully considered to ensure proper functionality of the MAX5079 ICs.

1) V_{BUS} is zero with a discharged capacitor (C_{BUS}). All three power supplies are turned ON simultaneously. V_{OUT1} comes up before V_{OUT2} and V_{OUT3}.

a. When V_{OUT1} turns on, the bus capacitors (C_{BUS}) begin charging from V_{OUT1} through N1's body diode. When V_{UVLO} (U1) rises above the UVLO threshold, the MAX5079 (U1) charge pump turns on, and U1 monitors the positive potential from V_{OUT1} to V_{BUS}. When $V_{OUT1} \geq V_{BUS}$ the charge pump brings GATE (U1) to 5.5V above V_{IN} (U1) (or 7.5V above V_{IN} depending on the magnitude of V_{IN}), by sourcing 2mA into N1's gate capacitance. This results in a less than 10µs turn-on time for the FDB7045L used in the MAX5079 evaluation kit. The fast turn-on is needed to assure that N1 is ON before the rising V_{OUT1} reaches its steady-state value. If the MOSFET is not turned on before V_{OUT1} reaches its steady state, V_{BUS} may overshoot due to the shorting of the 0.7V (forward drop) of N1's body diode. A higher V_{IN} (U1) can more quickly charge the charge-pump capacitor to 5V (or 7V), while a lower V_{IN} (U1) will take longer. Typically the MOSFET turns on at V_{GS} = 2.5V. Ensure that the soft-start time of the power supply is large enough (> 5ms) to avoid V_{OUT1} racing ahead and causing V_{BUS} to overshoot. Care must be taken to avoid the overloading of V_{OUT1} by either limiting the source current (using the current-sharing circuit) or delay the loading of the BUS until all three power supplies are up and running.

b. V_{OUT2} turns on and begins increasing the voltage at IN (U2). V_{UVLO} (U2) crosses the UVLO threshold, the MAX5079 (U2) charge pump turns on and U2 monitors the V_{OUT2} to V_{BUS} voltage. When this voltage difference becomes positive, GATE (U2) begins sourcing 2mA into N2's gate capacitance. During turn-on, the reverse voltage turn-off circuit is momentarily disabled. If V_{OUT2} is lower than V_{OUT1}, the external load-sharing controller circuit of PS2 will try to increase V_{OUT2} to source current from V_{OUT2}. Assume V_{OUT2}'s rise time is slow enough not to cause any overshoot before N2 turns on and starts sharing the current.

c. V_{OUT3} turns on and U3 follows the same sequence as U2. Eventually V_{OUT1}, V_{OUT2}, and V_{OUT3} reach to equilibrium and sharing equal currents.

2) PS1 and PS2 are on and sharing the load when PS3 is hot-inserted. PS3 will take the same course as discussed in 1b above.

a. If V_{OUT3} is higher than V_{BUS}, the BUS voltage will increase to the new level determined by V_{OUT3}. The external load-sharing controller circuit of PS1 and PS2 will increase V_{OUT1} and V_{OUT2} to force current sharing.

b. If V_{OUT3} is lower than V_{BUS}, the load-sharing circuit of PS3 will increase V_{OUT3} to force the sharing of current. This causes V_{OUT3} to increases above V_{BUS}. When this voltage difference becomes positive, GATE (U3) begins sourcing 2mA into N3's gate capacitance. Again, the reverse voltage turn-off circuit is disabled momentarily, as discussed before. The load-sharing circuit of PS3's controller will adjust V_{OUT3} so as to share the load current.

c. During the hot insertion, a voltage spike can occur at N1 and N2 and cause the (V_{OUT1} to V_{BUS}) or (V_{OUT2} to V_{BUS}) voltage to go negative. If the reverse voltage is below the fast-comparator reverse voltage threshold (V_{FTH}) but above the programmed slow-comparator reverse voltage threshold (V_{STH}), the spike is ignored for the programmed blanking time (t_{STH}). If the spike is longer than 50ns (the fast-comparator internal blanking time, t_{FBL}) and larger than V_{FTH}, then U1 and U2 will turn off N1 and N2 quickly. If the magnitude of the voltage spike is above V_{STH} but less than V_{FTH}, and longer than the slow-comparator blanking time (t_{STH}), U1 and U2 will turn off their respective ORing MOSFETs (N1 and N2) by discharging their GATE pins to PGND. The external load-sharing circuit of PS1 and PS2 will force V_{OUT1}, V_{OUT2} above V_{BUS} and N1, N2 will turn back on through the 2mA current sourcing from the GATE pins of U1 and U2. To avoid this situation the user can set the slow-comparator threshold and blanking time depending on the magnitude and duration of the voltage spikes.

d. PS3 fails to start. V_{UVLO} (U3) threshold is not crossed and U3 keeps N3 off.

e. PS3 goes into an overvoltage condition (no feedback). This causes V_{BUS} to go into an overvoltage condition increasing the loading on PS3 (provided PS3 is able to supply all the required BUS current). The current-sharing circuit will force the outputs of PS1 and PS2 to increase and eventually saturate at their current-sharing voltage range. Eventually only PS3 will have a positive voltage at IN (U3) with respect to BUS. PS1 and PS2 will have a negative voltage at V_{OUT1} and V_{OUT2} with respect to BUS. All overvoltage inputs OVI (U1), OVI (U2), and OVI (U3) sense the overvoltage, but only OVP (U3) is asserted and latched low. GATE (U3) is pulled to PGND and remains low as long as $V_{OVI} \geq 0.6V$. When V_{OVI} drops below 0.6V, OVP remains low. However, U3 tries to turn on N3 unless V_{OUT3} is actively kept below the undervoltage lockout. Use OVP (U3) to either drive the cathode of the optocoupler to shutdown PS3 from the primary side or use OVP (U3) to fire an SCR connected between V_{OUT3} and PGND.

3) PS1, PS2, PS3 are turned on with a shorted BUS.

Body diodes of N1, N2, and N3 conduct and short the outputs of PS1, PS2, and PS3 to PGND. The power supplies go into current limit (either in foldback or in hiccup mode). The MAX5079s remain in undervoltage lockout and keep all ORing MOSFETs off. The average current sourced by PS1, PS2, or PS3 must be low enough so as not to exceed the MOSFETs power dissipation ($P_D = V_F \times I_{SHORT}$).

a. Use additional n-channel MOSFETs in series with N1, N2, and N3 in the reverse direction to isolate the power supplies from a shorted bus (Figure 3). When power is turned on with a shorted bus, $V_{IN\_}$ (U1, U2, U3) increases and V_{UVLO} rises above the UVLO threshold. The MAX5079's GATE outputs start charging the back-to-back ORing MOSFET gates. The short-circuit condition at BUS collapses V_{IN} (U1), V_{IN} (U2), and V_{IN} (U3) sending the MAX5079s into undervoltage lockout. This turns off the MAX5079s entirely, including discharging of the charge-pump storage capacitors. The IN voltages come back up again crossing UVLO (UVLO has 60mV hysteresis). A new cycle starts and the time required to charge the charge-pump capacitor and the turn-on time of the device serves as a dead time. However, the dead time may not be enough to reduce the dissipation in the MOSFETs to an acceptable level. We advise in keeping the short-circuit current low and providing hiccup current-limit protection to the power supplies (PS1, PS2, and PS3).

b. Any other overload condition that would sustain the IN voltage above UVLO, will keep the MOSFETs ON continuously. Ensure the MOSFETs' current rating is higher than the maximum short-circuit source current of the power supplies (PS1, PS2, and PS3) to avoid damage to the ORing MOSFETs.

4) PS1, PS2, and PS3 are present and PS1 is shorted to GND.

V_{OUT1} drops below V_{BUS}. The negative potential from V_{IN} (U1) to V_{BUS} increases above the fast-comparator threshold and lasts longer than the 50ns blanking time. The MAX5079 (U1) takes its power from the voltage at BUS (U1). Connect BUS close to C_{BUS}, away from N1 so that U1 can receive power from BUS for a few microseconds until N1 isolates BUS from IN. N1 is discharged with 2A pulldown current, turning off N1 and isolating PS1 from the BUS. The load-sharing circuit of PS2 and PS3 will increase PS2 and PS3's load current until the total bus current requirement is satisfied.

For V_{IN} (U1) < 2.75V, V_{AUXIN} (U1) must come from an independent source or remain on for some time (a few microseconds) after V_{IN} (U1) has failed. This minimum on-time is needed to discharge the gate of the ORing MOSFET and isolate PS1 from the BUS.

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

5) PS1, PS2, PS3 are present and PS1 goes open.

PS1's output capacitors discharge and V_{OUT1} drops below V_{BUS}. The MAX5079 (U1) senses a negative potential from V_{OUT1} to V_{BUS}. Depending upon how fast PS1's output capacitor discharges, N1 is turned off due to the crossing of the fast- or slow-comparator reverse voltage threshold. N1's gate is discharged with a 2A sink current into GATE (U1), turning off N1 and isolating PS1 from the BUS. The load-sharing circuit of PS2 and PS3 will increase PS2 and PS3's load current until the total BUS current requirement is satisfied.

6) PS1, PS2, PS3 are present and providing BUS current. PS1 loses its feedback signal and goes into an overvoltage condition.

V_{BUS} increases and PS1 is loaded heavily. The current share circuit forces V_{OUT2} and V_{OUT3} higher and they will eventually saturate at their current-sharing voltage range. Now only PS1 has a positive voltage at IN (U1) with respect to BUS. All OVI inputs will sense the overvoltage, but only OVP (U1) will be asserted and latched low. GATE (U1) is pulled to PGND and remains low as long as $V_{OVI} \geq 0.6V$. When V_{OVI} drops below 0.6V, OVP remains low, however, U1 tries to turn on N1 unless V_{OUT1} is actively kept below the undervoltage lockout. Use OVP (U1) to either drive the cathode of an optocoupler to shutdown PS1 from the primary, or fire an SCR connected between IN (U1) and PGND.

Internal and External Undervoltage Lockout

The internal undervoltage lockout monitors V_{IN} and V_{AUXIN} and keeps the MAX5079 off until either voltage reaches 2.75V. Once powered and V_{IN} and/or V_{AUXIN} increase above 2.75V, the external UVLO is monitored. The external undervoltage lockout feature monitors the UVLO input and keeps the MAX5079 off (GATE shorted to PGND) until V_{UVLO} is greater than 0.66V. Connect a resistive divider from IN to UVLO to GND or from AUXIN to UVLO to GND to set the external undervoltage lockout threshold. We advise setting the external UVLO ≥ 2.75V when AUXIN is not present.

Charge Pump

The MAX5079 has an internal charge pump that pumps the gate-drive voltage (V_{GATE}) high enough to fully enhance the n-channel ORing MOSFET. The charge pump is divided into two stages, a voltage doubler running at 70kHz using an external charge-pump capacitor (C_{EXT}), and a voltage tripler running at 1MHz using an internal capacitor.

Connect an external capacitor (C_{EXT}) between C+ and C-. C_{EXT} is charged from the higher of V_{IN} or V_{AUXIN}. When the rising V_{IN} becomes greater then V_{BUS} (V_{UVLO} > 0.66V), C_{EXT} is discharged through GATE into the external MOSFET's gate capacitance. The charge-pump output is controlled by an internal regulator. The charge-pump output at GATE sources typically 2mA. This provides enough current drive to turn on a typical ORing MOSFET in less than 10µs. When (V_{GATE} - V_{IN}) reaches the target value (depending on V_{IN}) the charge pump is switched off (see the *Electrical Characteristics* table). Choose C_{EXT} equal to 10 times the ORing MOSFET gate capacitance. Too low of a capacitance will delay the turn-on of the ORing MOSFET, while too high of a capacitance can cause excessive ripple at V_{IN}. Bypass IN to GND with a 1µF ceramic capacitor to avoid ripple at IN caused by the charge-pump switching. A clamp is placed internally between GATE and IN to prevent (V_{GATE} - V_{IN}) from exceeding 11V. When V_{IN} is less than 5V, the charge pump (tripler) will increase V_{GATE} to 3x's V_{IN} to further reduce the R_{DSON} of the ORing MOSFET. The internal charge-pump booster (voltage tripler) section is operational only when V_{IN} and V_{AUXIN} are low and is turned off when V_{IN} exceeds 5V.

When an additional supply is connected to AUXIN and (V_{AUXIN} - V_{IN}) > 5V, both charge pumps are completely disabled. In this case, the charging of the ORing gate comes entirely from V_{AUXIN}. In this case, the charge-pump flying capacitor can be eliminated and C+, C- can be left floating.

GATE Drive and Gate Pulldown

The MAX5079's charge pump provides bias to charge the ORing MOSFET gate above IN (the MOSFET's source). GATE source current and the turn-on speed depends upon the value of C_{EXT} (connected between C+ and C-). Typically GATE can source up to 2mA with C_{EXT} = 0.1µF. This enables V_{GATE} to rise to over 2V above V_{IN} in less than 10µs for an ORing MOSFET gate capacitance of up to 10nF. With V_{IN} < 5V, 12V MOSFETs can be used for better R_{DSON} characteristics. The MAX5079 automatically selects the gate-drive voltage for

V_{IN} = 5V or V_{IN} = 12V. For $V_{IN} \le 8V$, the gate drive is 5V above V_{IN} and for $V_{IN} > 8V$, the gate drive is 7V above V_{IN}. Lower gate drive means faster turn-off during faults, while higher gatedrive means lower R_{DSON}.

A fast and slow comparator monitor the voltage from IN to BUS. When this voltage crosses the negative fast- or slow-comparator threshold voltage for the blanking time duration, GATE is pulled low by an internal 2A current sink. Both comparators have an adjustable threshold voltage. GATE is pulled low if any of the following conditions are met.

1) $V_{UVLO} < 0.6V$.

2) $V_{AUXIN} < 2.25V$ and $V_{IN} < 2.25V$.

3) $V_{OVI} \ge 0.6V$.

4) $V_{IN} \le (V_{BUS} - V_{FTH})$ or $V_{IN} \le (V_{BUS} - V_{STH})$ and $(V_{GATE} - V_{IN}) \ge 1.8V$.

When the above conditions are not true and $V_{IN} \le V_{BUS}$, GATE is shorted to IN. To insure that the external MOSFET is quickly turned off, given the above conditions, the GATE pulldown circuitry is powered by either V_{IN}, V_{AUXIN}, or V_{BUS} as long as any one is greater then 2.75V.

Fast Comparator (FTH)

The fast comparator has a 50ns blanking time to avoid unintentional turn-off of the ORing MOSFET during fast transients. Additionally, the fast-comparator reverse voltage threshold (V_{FTH}) is programmable to suit the need of an individual application. Higher V_{FTH} threshold allows for a larger glitch at BUS during a fault, but improves the noise immunity. Lower V_{FTH} reduces glitches at BUS during a fault, however, with lower V_{FTH} spikes at BUS or glitches at IN can be read as faults, unintentionally turning off the ORing MOSFET. Program V_{FTH} by connecting a resistor from FTH to GND. Adjust V_{FTH} to optimize the system performance using the following equation:

$$R_{FTH} = \frac{V_{FTH} - 24mV}{6.67\mu A}$$

V_{FTH} can be chosen from 24mV to 400mV. Connect FTH to GND to choose the default 24mV threshold.

Slow Comparator (STH)

The MAX5079 includes a slow comparator to provide glitch immunity during the hot insertion or removal of paralleled power supplies. During the hot insertion, BUS can see voltage spikes. These spikes can be interpreted as a reverse voltage across the ORing MOSFET. The amplitude of the spikes is proportional to the load step seen by the parallel power supply while the duration of the spikes depends on the loop response of the load share and PWM controller.

The slow comparator has a programmable reverse voltage threshold (V_{STH}) as well as a programmable blanking time (t_{STH}). An internal transconductance amplifier converts the IN to BUS differential voltage to a current and applies it to a parallel combination of resistor and capacitor (R_{STH} and C_{STH}) from STH to GND. The reverse threshold voltage (V_{STH}) for the slow comparator is adjusted through R_{STH}. Use the following equation to calculate the R_{STH} for a required V_{STH}.

$$R_{STH} = \frac{1V}{(V_{STH} - 12mV) \times G_{M\_STH}}$$

where G_{M_STH} = 0.17mS.

The internal 500kΩ resistance from the output of the transconductance to GND can change the actual V_{STH} if R_{STH} is above 50kΩ. In this case, see the *Typical Operating Circuit* to select R_{STH}. Once R_{STH} is chosen, the blanking time can be adjusted by C_{STH}. The delay time is:

$$t_{DELAY} = R_{STH} \times C_{STH} \times \left[-\ln\left(1 - \frac{V_{STH}}{V_{STH} + V_{DD}}\right)\right] + t_{SBL}$$

where t_{SBL} = 0.9ms and is the default blanking time generated by an internal digital delay. Leaving STH floating results in a 12mV threshold voltage and a 0.9ms blanking time. V_{OD} (overdrive) is the difference between actual reverse voltage (V_{BUS} - V_{IN}) and V_{STH} threshold.

Overvoltage Protection Latch (OVI/OVP)

OVI is the negative input to the overvoltage comparator. The positive input of this comparator is connected to the internal 0.6V reference and an open-drain output is provided at OVP. The overvoltage sensing for overvoltage protection is done at either IN or BUS. OVP

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

latches low and the internal GATE pulldown circuitry is activated and pulls GATE low only when both of the conditions are satisfied:

1) $V_{OVI} \geq 0.6V$.

2) $V_{IN} \geq V_{BUS}$.

OVP can sink 10mA maximum. Cycle power or pull UVLO low and then high again to reset the OVP latch. GATE is pulled to PGND and remains low as long as $V_{OVI} \geq 0.6V$. When V_{OVI} drops below 0.6V, OVP remains low. However, the MAX5079 tries to turn on the ORing MOSFET unless V_{IN} is actively kept below the undervoltage lockout. Use OVP to drive the cathode of an optocoupler to shut down the respective power supply from the primary side (see the *Typical Application Circuit* of Figure 2) or fire an SCR connected from IN to PGND.

Power-Good Comparator (PGOOD)

PGOOD output pulls low when V_{UVLO} falls below 0.6V or V_{OVI} goes above 0.6V. PGOOD can sink a maximum of 2mA.

Layout Guidelines

1) Place a 1µF ceramic input bypass capacitor physically close to IN and PGND. Connect IN as close as possible to the source of the ORing MOSFET.
2) Sense the V_{BUS} close to the bulk capacitor, away from the drain of the ORing MOSFET. When IN is shorted to ground during a fault, BUS is also pulled low through the ORing MOSFET. In the absence of V_{AUXIN}, the MAX5079 loses both power inputs V_{IN} and V_{BUS}. This can cause a delayed pulldown of the gate. Sensing the BUS away from the ORing MOSFET drain, close to the BUS bulk capacitor provides power to the MAX5079 for a few microseconds, long enough to pull down the ORing MOSFET gate and isolate BUS from a shorted IN.
3) Place the charge-pump capacitor (C_{EXT}) and the slow-comparator blanking time adjustment capacitor (C_{STH}) as close as possible to the MAX5079.
4) Run a thick trace from the gate of the ORing MOSFET to GATE.

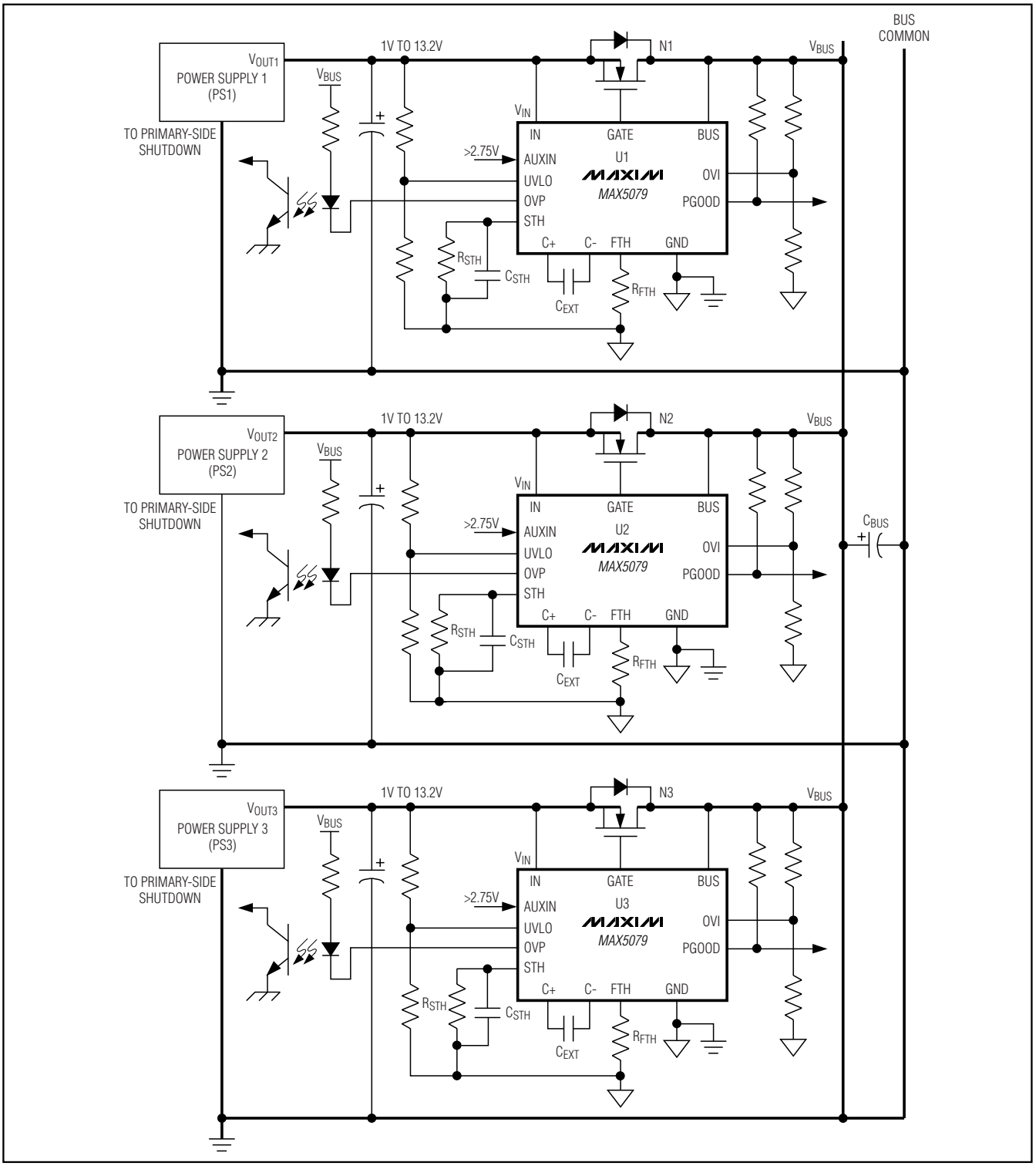


Figure 2. Typical Application Circuit

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

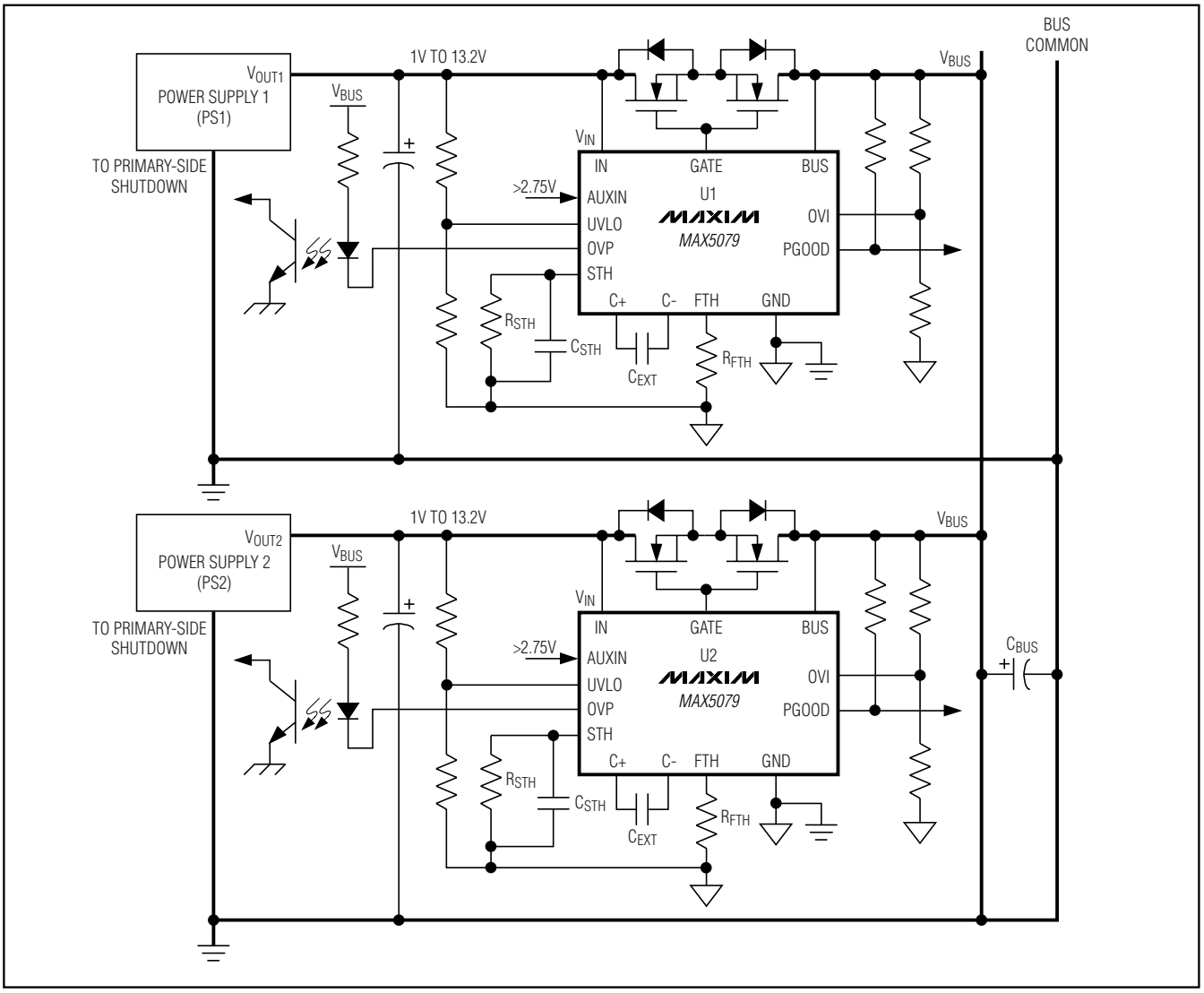
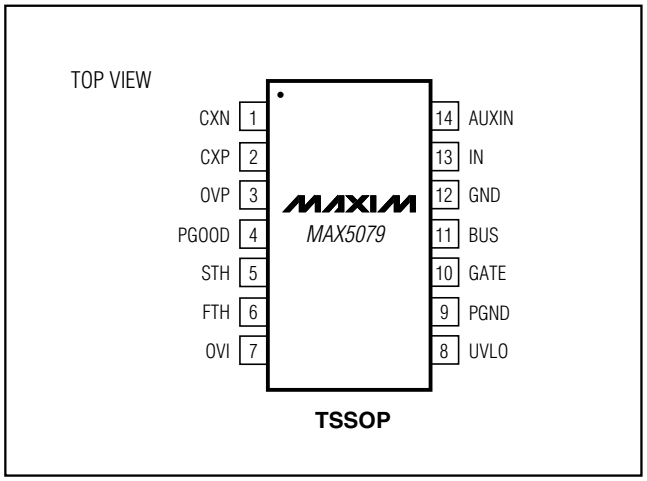


Figure 3. Parallel Supplies with Back-to-Back MOSFET

Pin Configuration



TSSOP

Chip Information

TRANSISTOR COUNT: 2,911

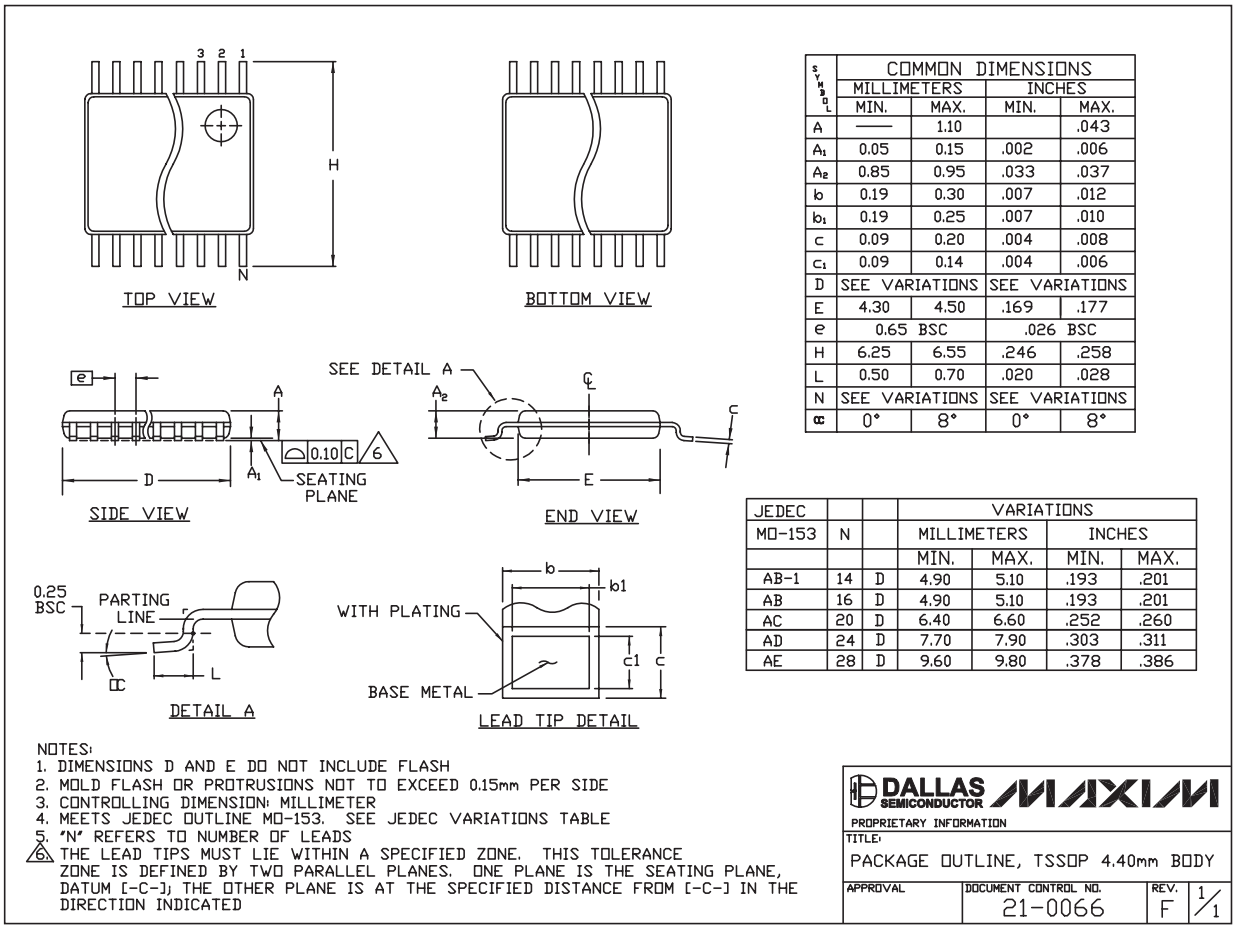
PROCESS: BiCMOS

ORing MOSFET Controller with Ultra-Fast 200ns Turn-Off

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1